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Design & Implementation of Various VERILOG Multipliers for Filters Computation for Biomedical Applications

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ABSTRACT

The digital finite impulse response (FIR) is widely practiced in many digital signal processing (DSP) systems, ranging from wireless communication to image and video processing. Digital FIR filter is mainly composed of multipliers, adders and delay factors. Various techniques have been described in the open literature to implement digital FIR filters using Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). Discrete Fourier Transform (DFT) is a fundamental Digital Signal Processing domain transformation technique used in many applications for frequency analysis and frequency domain processing. Fast Fourier Transform (FFT) is utilized for signal processing applications. It consists of addition and multiplication operations, whose speed improvement will enhance the accuracy and performance of FFT computation for any This reduces computation time by various orders of magnitude and the improvement is roughly proportional to N / log N. Present day Research focus is on performance improve

Computation of FFT specific to field of application. Many performance improvement studies are in progress to implement efficient FFT computation through better performing multipliers and addersElectroencephalographic (EEG) signals are always utilized for clinical diagnosis and conventional cognitive neuroscience. This study intends to lead to a faster method of computation of FFT for the analysis of EEG signals to classify Autistic data.

Keywords:—FIR, FFT, Multiplier, EEG

I. INTRODUCTION

Modern applications are demanding high speed computations. Applied science is performing close to theoretical limits on how fast computations can be taken out on a single microchip. Multiple processors operating in parallel, performing different functions of a process and mixing them at the end are the solution to this. Fourier Transform is the foundation of many signal processing and communication applications. It is the tool for analysis of the signal in its frequency domain. Fourier transform has many applications, in fact any field of physical skill that uses varying signals, such as applied science, natural philosophy, applied math, and chemistry, will make use of Fourier series and Fourier transforms. Most of these fields nowadays make use of digital and discrete data. Hence the determination of Fourier Transform of discrete signals are of prime importance and such a transform is called Fast Fourier Transform (FFT) is an efficient algorithm to evaluate DFT. Discrete Fourier Transform has a wide range of applications. It is mainly used for converting discrete time domain signals to its frequency domain. However, the mental process of conversion is expensive and takes a great sight of time. Then we go for Fast Fourier Transform which uses a divide-and-conquer approach to reduce computational complexity of DFT. DFT is defined as Discrete Fourier Transform (DFT). Where n, k € [0, N-1] and $W^{K} = e^{-j2}\prod^{k/N}$ is the twiddle factor, x (n)
Is the net sample of discrete time signal and
X (k) is its frequency sample at kit instant.

Complexity of computation of DFT is O (N^2) unlike the computation of FFT which is O (N log N) butterfly operations. Hence DFT computation takes more time and is a costly process. FFT algorithm deals with these complexities by exploiting regularities in the DFT algorithm. Radix-2 Algorithm is a common factor algorithm for N-point DFTs, where N is a power of 2. FFT computation in the Radix-2 system takes place in log2N different steps, so it enables pipelining in hardware design.

FFT computation involves addition and multiplication operations. As multipliers are slow performing hardware units, their performance directly affects the operation of the FFT hardware. Existing hardware multipliers are Serial Multiplying, Array Multiplier, Booth Multiplier, Wallace Tree Multiplier, Booth encoded Wallace tree multiplier, etc. Studies on performance optimizations of Booth Multiplier, Wallace Tree Multiplier and Booth encoded Wallace Tree Multipliers are in progress. Forward movement in terms of Hardware Description Language (HDL), Floor planning, Routing, etc. are of primary interest to Researchers. This study intends to compare the operation of main hardware multipliers and study and implement the most efficient multiplier for FFT computations in the biomedical domain.

Filters are extensively applied in data compressions, Filtering signals, Signal spectral

analysis, Image Processing, Electroencephalography (EEG) and electrocardiography (ECG) are diverse techniques to examine the forms of signal functions. This work analyses spectral components of EEG signals and proposes an effective method to classify EEG Plasma fatty acid levels in autistic children.

II. FAST FOURIER TRANSFORMALGORITHM FOR FILTERS DESIGNING

Fast Fourier Transform is an algorithm to compute Discrete Fourier Transform which diminishes the number of computations for n-point radix from N^2 to N long arithmetic operations. There are two methods to compute the DFT through FFT algorithm, namely, Decimation-in- time (DIT) and Decimation-in-frequency (DIF) FFT algorithms. In Radix-2 DIT-FFT, the input signal is decimated into even-indexed and odd-indexed values such that the series x (n) where, in=0, 1,2,… N changes to x (2r) and x (2r+1) where are=0,1,2,…. N/2-1. In Radix-2 DIF- FFT, the x (n) series is broken into x (n) for n=0,1,2…. N/2 -1 and x (n) for an=N/2, N/2+1,…. N-1.

MULTIPLIERS

Multipliers have large area, long propagation delays and waste power. Thus, low-power multiplier design has a strong part in the design of low-power VLSI systems. Ability refers to the number of Joules dissipated over a certain amount of time, whereas energy is the sum of the total number of Joules dissipated by a circuit [9]. In digital CMOS design, the generated by brain and nerve, respectively. These are further subdividedWell-known power-area/power-delay product is commonly applied to appraise the merits of the designs [9].

Any multiplier design involves 3 steps. They are i) partial product generation ii) partial product reduction and addition iii) final edition. The partial products are formed first either by applying an algorithm or using AND gate for each piece of the multiplier with each piece of the multiplicand. The following step is reduction of these partial products. The third step is the summation of the remaining partial products to generate the final product [9].

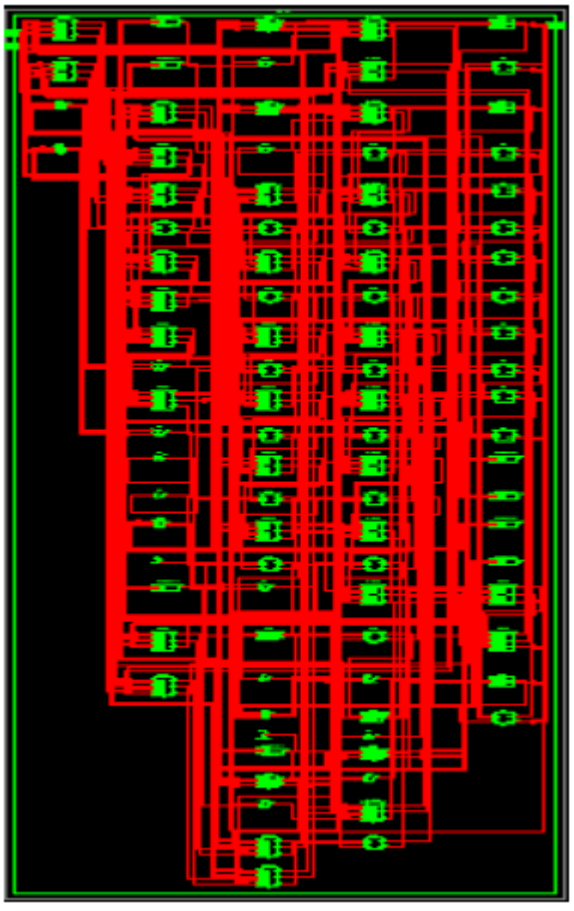
Hardware multipliers widely used are Booth Multipliers and Wallace Tree Multiplier. Field and Power parameters of Booth Multiplier and Wallace Tree Multiplier are studied and their advantages have been integrated to acquire the concept of Booth-encoded Wallace Tree Multiplication.

A. Booth Multiplier

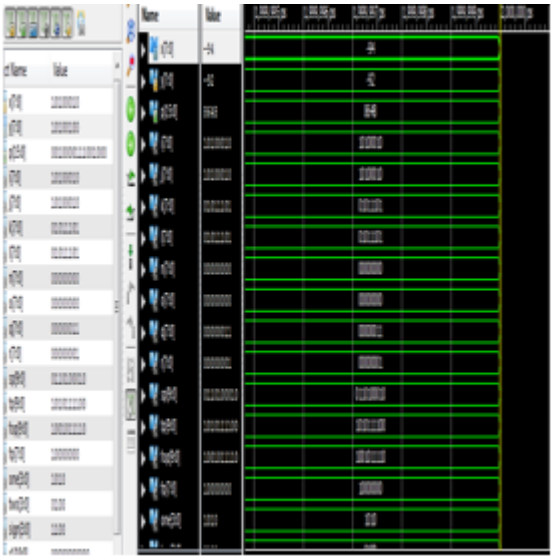
Booth Multiplier implements Booth Algorithm, named after its originator, A. D. Kiosk. This algorithm is implemented for signed multiplication of integers and can be extended to real numbers. The algorithm is based on laying down the multiplier to a recorded value, leaving the multiplicand unchanged [6] i.e.

- Each '0' digit is retained in the recorded number until 1 is encountered in evaluating from LSB to MSB.
- Complement of 1 is inserted at every '1' digit in recorded number and all other succeeding 1's are complemented by a '0' is encountered.
- Then, replace the '0' with '1' and continue the procedure.

Two main drawbacks of Booth Algorithm are the inefficiency of the circuit when isolated 1's are encountered and difficulty in designing parallel multipliers as number of shift-and-add operations may vary. Hence Modified Booth Algorithm was developed by O. L. Macsorley. Modified Booth Algorithm is twice as fast as normal Booth Algorithm [4]. This modified Booth Encoding algorithm reduces the number of partial product rows to (N +2) /2 where N is the number of pieces of the Multiplier



RTL of Booth Multiplier



Output of Booth Multiplier

B. Wallace Tree Multiplier

Wallace Tree Multiplier is one of the hardware multipliers used to achieve high velocity and low power multiplication to condense the number of partial products generated. There are two main techniques followed in designing Wallace Tree Multiplier. The first technique is to think all bits in each pillar at a time and compress them into two sections, namely, Sum and Carry. The second technique is to think all bits in four classes at a time and push them. Wallace Tree Multipliers use half adder, full adders, 4:2 and 3:2 compressors and a high speed adder [10].

Partial product generation, partial product addition and final edition are the three stages in a multiplier. In Wallace Tree Multiplier, the multiplicand is multiplied by the multiplier, bit- by-bit, to generate partial products. They are, then, added based on Wallace Tree structure to bring around two rows of partial products which are finally added using any high speed adder. The critical path delay of Wallace Tree multiplier is Proportional to the logarithm of the number of bits in the multiplier [9].

An algorithm for Multiplication of two signed integers is as follows:

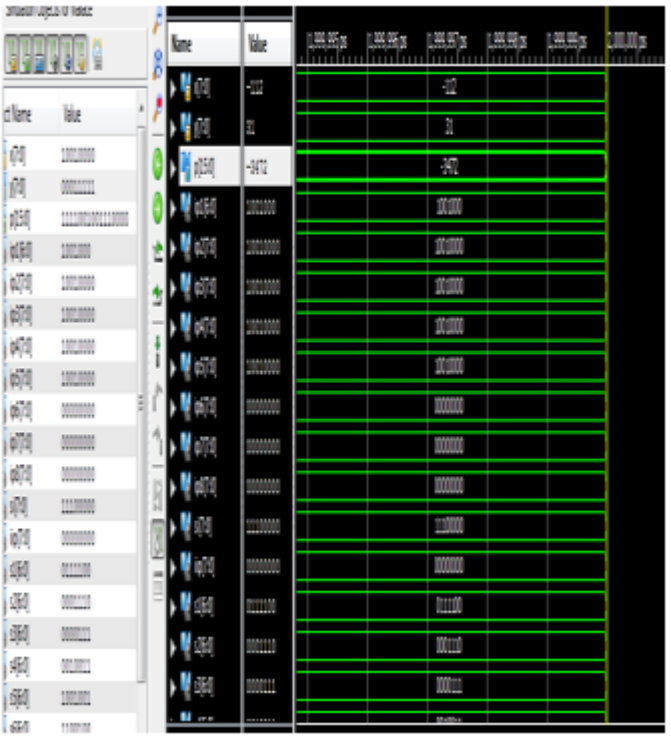
• Multiply (AND) each bit of one of the creases,

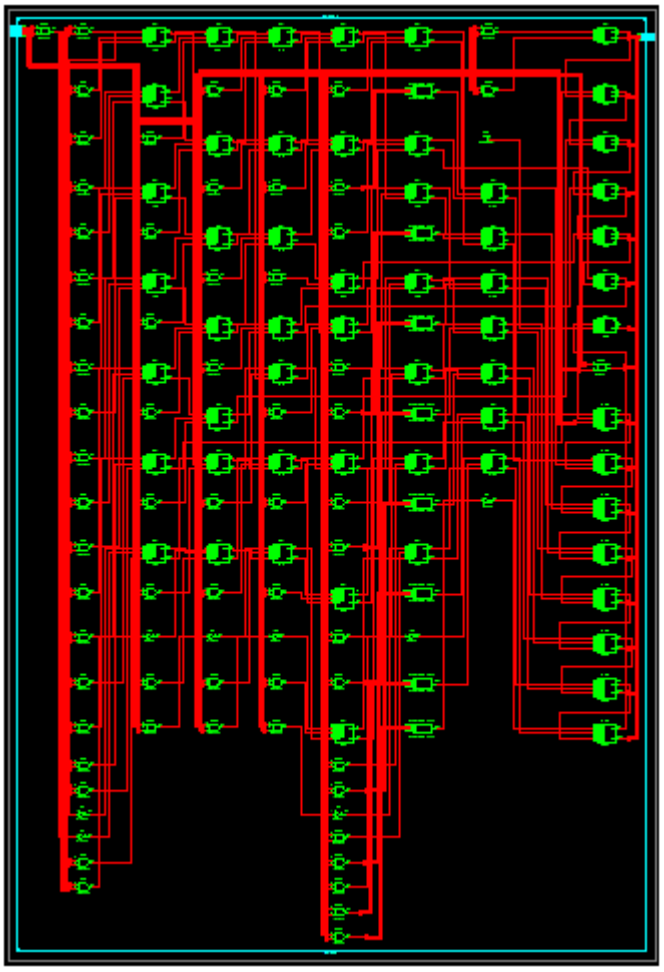
• Reduce down the number of partial products in two by layers of full adders and half adder (Compressors).

• Group the wires in two numbers, and add them with a conventional adder [9].

Wallace tree multiplication can be carried out only for signed integers and are avoided for low power applications as excess wiring consumes more power.

Output of Wallace Tree Multiplier





RTL Diagram of Wallace Tree Multiplier

C. Hybrid Multiplier

Based on the comparative study of Area and Power parameters of Booth Multiplier and Wallace Tree Multiplier, Booth-encoded Wallace Tree Multiplier is chosen as an efficient multiplier for FFT computation.

Table I. Shows Area and Power performance parameters of the two multipliers which are coded in Verilog HDL and performance parameters Are evaluated using IC Compiler tools from Synopsys Inc. Though Wallace Tree multiplier shows better performance in terms of Area and Power than the Booth multiplier, its execution is limited to signed integers alone. As FFT computation in biomedical applications involve signed real numbers, Booth Algorithm is to be put through for the multiplier.

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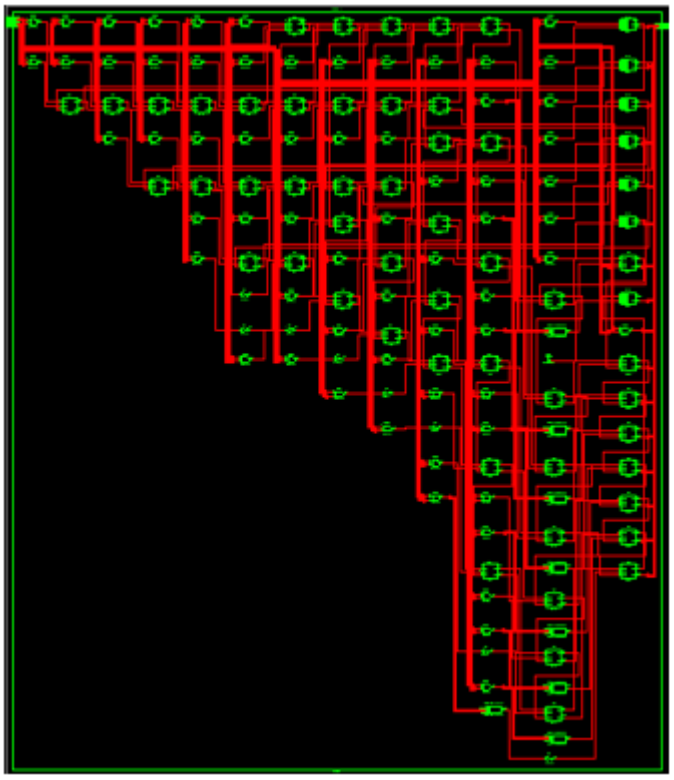
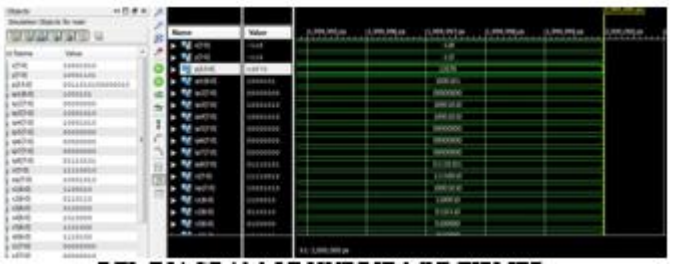


RTL DIAGRAM OF HYBRID MULTIPLIER



RTL DIAGRAM OF HYBRID MULTIPLIER

Selecting partial products from the set {0, M, 2M, 3M} where M is the multiplicand. Modified Booth encoded multiplier, avoids the employment of the Carry Propagate Adder to calculate 3M, rather it utilizes Carry-Save-Adder. Hence, in Modified Booth Algorithm, the number of partial products is scaled down by a ingredient of two without a pre-adder to produce partial products [6]. Multiplier decoding is done such that multiples needed are in {0, M, 2M, 4M + -M} data set.
These multiples can be generated using shift-and-complement methods.

Wallace Tree Multiplier which consists of five blocks, namely, 2's Compliment Generator, Booth Encoder, Partial Product Generator, Wallace Tree module and Carry Look- ahead Adder [7]. Booth encoder inspects each bit of the multiplicand and records the multiplier in terms of 0, 1 and complement of 1. . As complement of 1 cannot be represented In hardware, operating equivalent of recorded multiplier is implemented based on Table II. Here, outputs of the encoder. X and z are defined

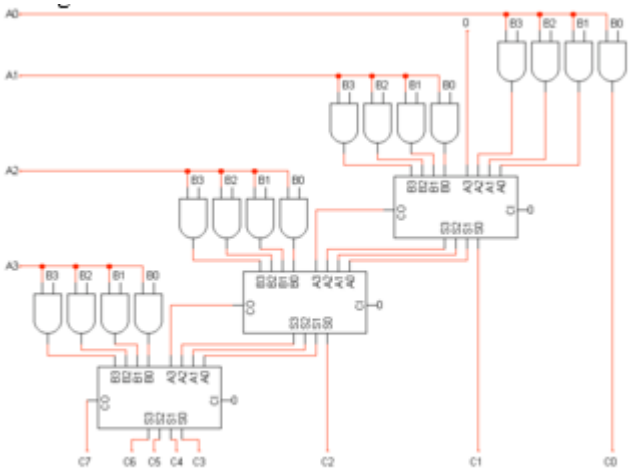
$$X \square MR[I] \square MR[I \square 1] \quad (2)$$

$$Z \square MR[I] \square MR[I \square 1] \quad (3)$$

TABLE I. PERFORMANCE PARAMETERS OF 4X4 BOOTH MULTIPLIER AND WALLACE TREE MULTIPLIER

Multiplier	Area(nm^2)	Power(µW)
Booth Multiplier	958.872	265.86
Wallace Tree Multiplier	590.868	140.45

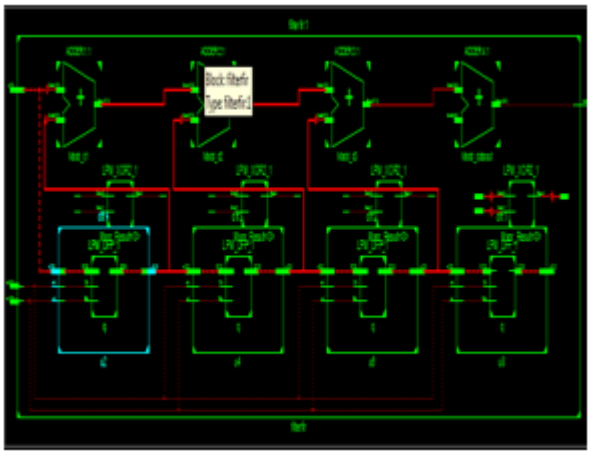
Multiplication of the two operands, Multiplicand (MD) and Multiplier (MR) results in 2N bits for conventional generation. Still, Booth encoded multiplier reduces the number of partial products to (MD/2 -1) partial products [5]. Booth Algorithm is based on putting down the multiplier to a recorded value, leaving the multiplicand unchanged. It scans the multiplier operand and skips chains. It cuts the number of additions required to create the solution [4]. Booth-encoded Wallace Tree Multiplier has advantages of both Booth Multiplier and Wallace Tree Multiplier. This paper implements Booth encoding to increase speed of algebra by reducing the



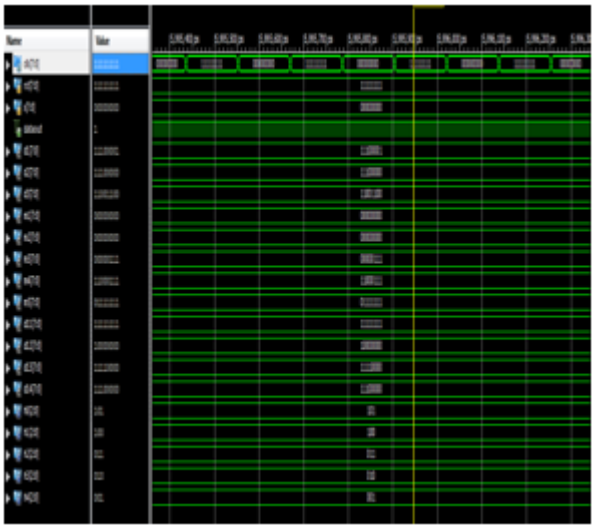
Number of partial products and Wallace Tree module for decreasing number of levels of addition.

1) Architecture of the Multiplier

In Booth encoded multiplier, the number of partial products is scaled down by grouping multiplier bits into pairs and Where MR [I] and MR [I-1] corresponds to it and an I-1th bit of the Multiplier, respectively. 2's complement generator takes the multiplicand MD as input and produces –MD as output. I. e. Inverts all bits of the multiplicand and uses a Ripple Carry Adder to generate 2's complement. Partial product generator generates appropriate partial products to be added to the Wallace tree structure. The Wallace Tree module adds all partial products. Addition is implemented using Carry Look Ahead Adder [7].



RTL of FIR Filter



Output of FIR Filter

TABLE II. BOOTH ENCODING VALUES

MR [I]	MR [I-1]	Put down Y [I]	x	z	Assigned to partial Product
0	0	0	0	0	0
0	1	1	0	1	MD. sign extended
1	0	1.	1	1	-MD, sign extended
1	1	0	0	0	0

Hardware Description Language (HDL) implementation of Booth-encoded Wallace Tree Multiplier has been done in Verilog HDL. The end products are correctly obtained for both signed and unsigned multiplication. Simulation has been done using Xilinx ISE tool. Generic Gate-level schematic has been obtained in IC Compiler tool from Synopsys Inc. Fig. 3 and Fig. 4 show the simulation effects and Generic Gate-level Schematic of the Booth-encoded Wallace Tree Multiplier.

FFT WITH BOOTH-ENCODED WALLACE TREE MULTIPLIER

The multiplier is an efficient circuit with advantages of both Booth Multiplier and Wallace Tree Multiplier. As explained in II, Modified Booth Algorithm is applied to calculate Partial Products as per Table II. Partial Product Generator provides minimum The number of partial products which are added using Wallace structure. Hence, efficient algorithm of multiplication is implemented.

FIR Filter has been coded in Verilog HDL for input values scaled up by a factor of 10000. There are ten inputs to the circuit, namely, eight time-domain samples, Twiddle factor 'wr' and the scaling factor 'k'. The end products are separately obtained for material and imaginary parts of corresponding frequency components.

As 8-point corresponds to 3 points (8 = 23), twiddle factor varies for each phase.tage. Twiddle factor is calculated as

in (1). For N=1, Twiddle factor value is {1}, for N=2, Twiddle factor values are {1, -j} and for N=3, Twiddle factor values are {1, -j, (1/ 2) – j (1/ 2), (-1/ 2) - j (1/ 2)}. Depending on the accuracy of outputs required, scaling can be altered from 10 to any power of 10 and by increasing the number of significant digits of the twiddle factor value of (1/ 2). Models and simulation solutions are presented Shown in Fig.5 has been scaled up for a factor of k = 10000. Outputs and inputs have been
Correctly verified. Accuracy of information □ 0.1% is
Obtained for scaling improvement from 1000 to 10000.

Design Vision tool Xillinx is a logic synthesis tool which inputs HDL design and synthesize out gate- level HDL net lists.

III. RESULTS AND DISCUSSION

EEG data collected from a normal person have been sampled at 80 Hz in MATLAB. Delta band value X0 has been obtained as -0.0006526 volts. FIR has been implemented using Booth- encoder Wallace Tree multiplier to compute Filtering algorithm. The same sample has been given as input to the FFT circuit in Test bench and delta band value is obtained as (-55270000 x $10^{\wedge -10}$) volts.4% has been experienced through the implemented FIR circuit for all eight outputs obtained.

IV. CONCLUSION AND FUTURE SCOPE

Generic-gate level implementation of Fast Fourier Transform using Booth-encoder Wallace Tree Multiplier has been done using VLSI 90nm technology. The circuit has been studied and analyzed for data accuracy and efficiency performance. been got for four decimal places of twiddle factor (1/ 2).. By increasing the number of significant digits of the twiddle factor, accuracy of the output can be improved, but it will share a trade-off with the expanse of the circle. Physical level chip design and further optimization of the circuit in terms of area and power and increasing the number of points for FFT computation from the future scope of use.

Autistic EEG samples can be evaluated for the mid- frequency alpha band. This value is required to be more depressed than normal person [1]. This circuit can therefore be used to classify Autistic people based on EEG level and this work can be extended for its further analysis and verification.

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